

N-channel 650 V, 0.475 Ω typ., 8.5 A MDmesh™ V Power MOSFET in a PowerFLAT™ 5x6 HV package

Datasheet – production data

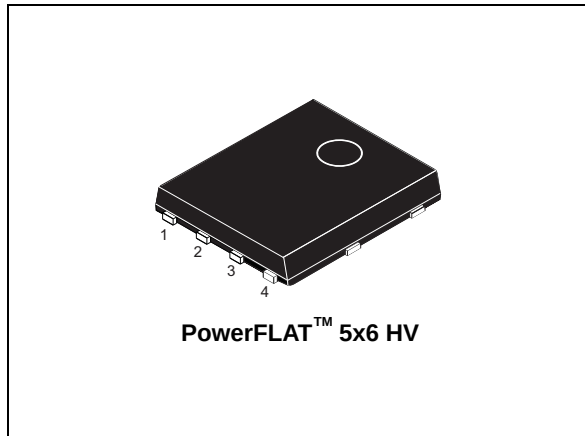
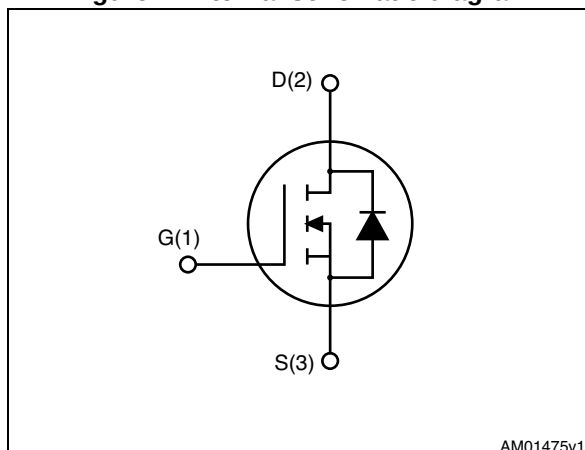


Figure 1. Internal schematic diagram



Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STL12N65M5	710 V	0.530 Ω	8.5 A

- Outstanding R_{DS(on)}* area
- Extremely large avalanche performance
- Gate charge minimized
- Very low intrinsic capacitance
- 100% avalanche tested

Applications

- Switching applications

Description

This device is an N-channel MDmesh™ V Power MOSFET based on an innovative proprietary vertical process technology, which is combined with STMicroelectronics' well-known PowerMESH™ horizontal layout structure. The resulting product has extremely low on-resistance, which is unmatched among silicon-based Power MOSFETs, making it especially suitable for applications which require superior power density and outstanding efficiency.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL12N65M5	12N65M5	PowerFLAT™ HV	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	650	V
V_{GS}	Gate-source voltage	± 25	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^{\circ}\text{C}$	8.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^{\circ}\text{C}$	4	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	34	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^{\circ}\text{C}$	48	W
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_j max)	1.9	A
E_{AS}	Single pulse avalanche energy (starting $T_j = 25\text{ }^{\circ}\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$)	130	mJ
$dv/dt^{(3)}$	Peak diode recovery voltage slope	15	V/ns
T_{stg}	Storage temperature	- 55 to 150	$^{\circ}\text{C}$
T_j	Max. operating junction temperature		$^{\circ}\text{C}$

1. Limited by maximum junction temperature

2. Pulse width limited by safe operating area.

3. $I_{SD} \leq 8.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$, $V_{Peak} \leq V_{(BR)DSS}$, $V_{DD} = 400\text{ V}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.6	$^{\circ}\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	59	$^{\circ}\text{C}/\text{W}$

1. When mounted on 1inch² FR-4 board, 2 oz Cu.

2 Electrical characteristics

($T_C = 25\text{ }^{\circ}\text{C}$ unless otherwise specified)

Table 4. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ($V_{GS} = 0$)	$I_D = 1\text{ mA}$	650			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 650\text{ V}$			1	μA
		$V_{DS} = 650\text{ V}$, $T_C = 125\text{ }^{\circ}\text{C}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 4.25\text{ A}$		0.475	0.530	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	644	-	pF
C_{oss}	Output capacitance		-	18	-	pF
C_{rss}	Reverse transfer capacitance		-	2.5	-	pF
$C_{o(tr)}^{(1)}$	Equivalent capacitance time related	$V_{DS} = 0\text{ to }520\text{ V}$, $V_{GS} = 0$	-	55	-	pF
$C_{o(er)}^{(2)}$	Equivalent capacitance energy related		-	17	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	Ω
Q_g	Total gate charge	$V_{DD} = 520\text{ V}$, $I_D = 4.5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	17	-	nC
Q_{gs}	Gate-source charge		-	4.6	-	nC
Q_{gd}	Gate-drain charge		-	8.5	-	nC

1. $C_{oss\text{ eq}}$ time related is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}
2. $C_{oss\text{ eq}}$ energy related is defined as a constant equivalent capacitance giving the same stored energy as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS}

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_d(v)$	Voltage delay time	$V_{DD} = 400\text{ V}$, $I_D = 6\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 17), (see Figure 20)	-	23	-	ns
$t_{r(v)}$	Voltage rise time		-	10	-	ns
$t_{f(i)}$	Current fall time		-	13.5	-	ns
$t_{c(off)}$	Crossing time		-	13	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}^{(1)}$	Source-drain current		-		8.5	A
$I_{SDM}^{(1),(2)}$	Source-drain current (pulsed)		-		34	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 8.5\text{ A}$, $V_{GS} = 0$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 8.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see Figure 17)	-	232		ns
Q_{rr}	Reverse recovery charge		-	2		μC
I_{RRM}	Reverse recovery current		-	17.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 8.5\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$ (see Figure 17)	-	328		ns
Q_{rr}	Reverse recovery charge		-	2.8		μC
I_{RRM}	Reverse recovery current		-	17		A

1. Limited by maximum junction temperature
2. Pulse width limited by safe operating area
3. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

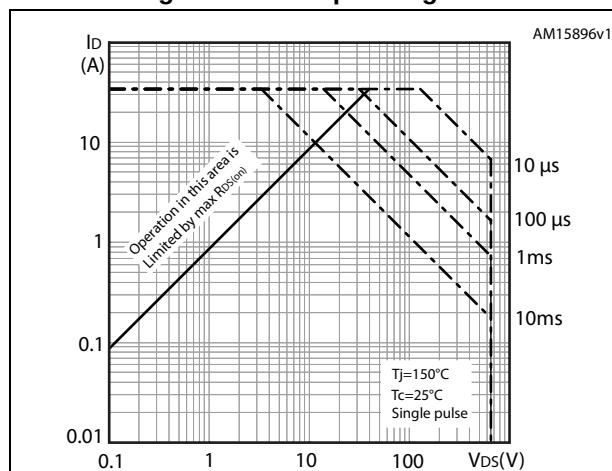


Figure 3. Thermal impedance

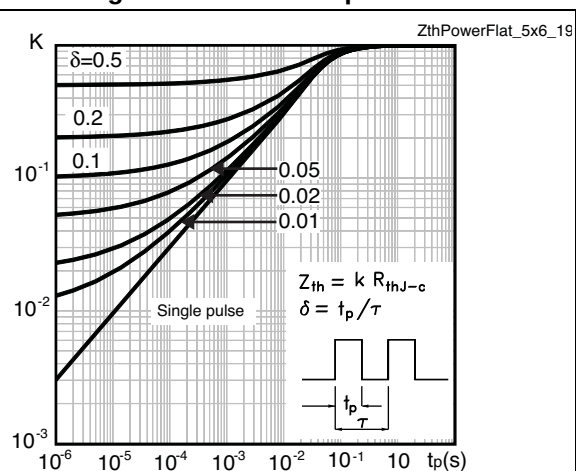


Figure 4. Output characteristics

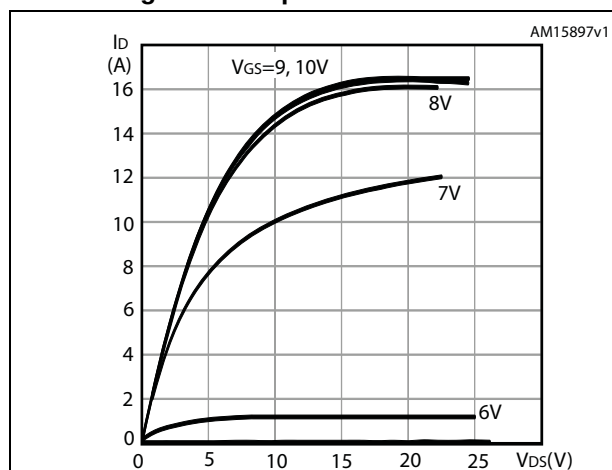


Figure 5. Transfer characteristics

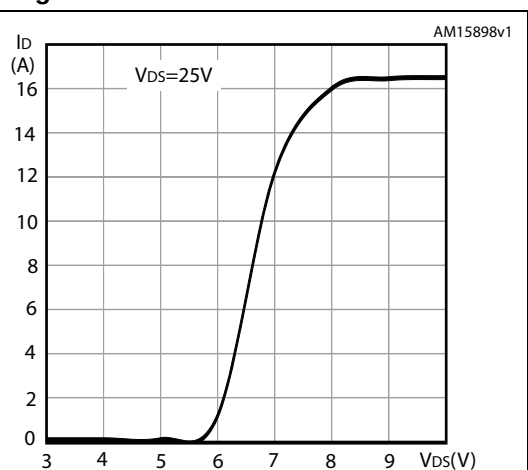


Figure 6. Static drain-source on-resistance

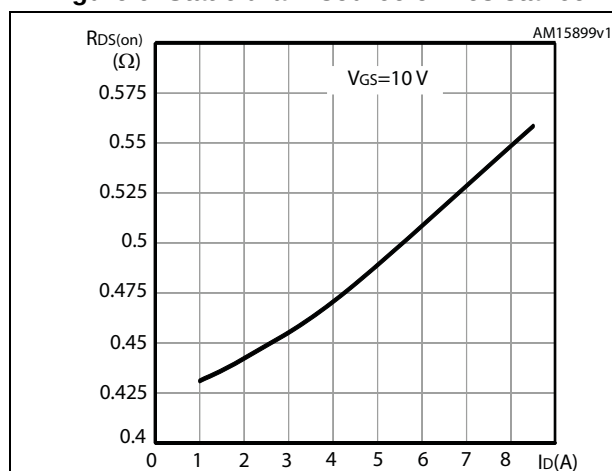


Figure 7. Gate charge vs gate-source voltage

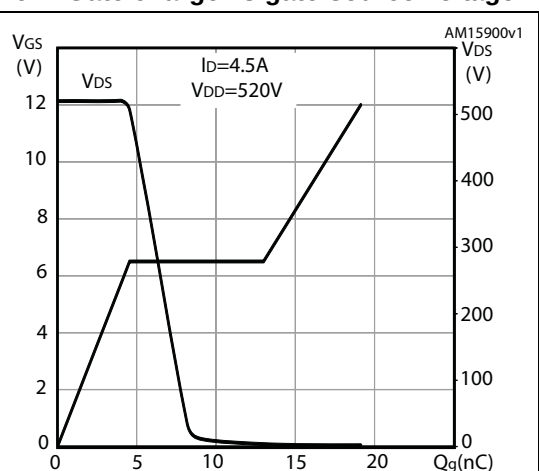


Figure 8. Capacitance variations

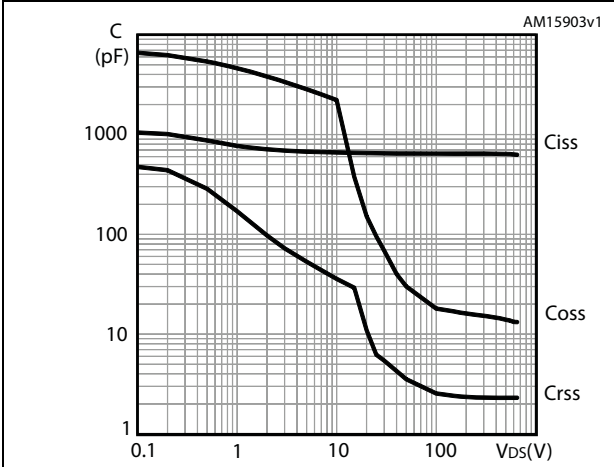


Figure 9. Output capacitance stored energy

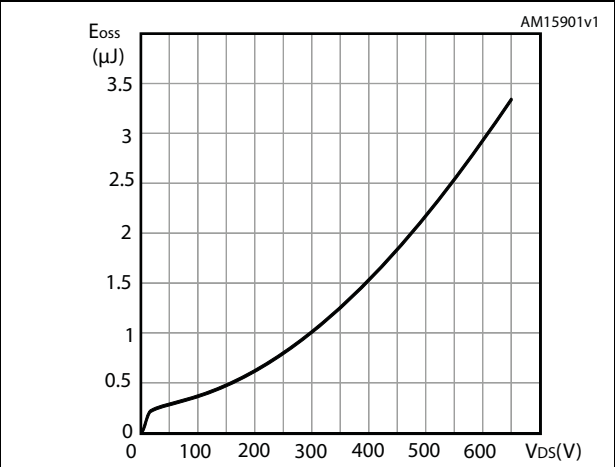


Figure 10. Normalized gate threshold voltage vs temperature

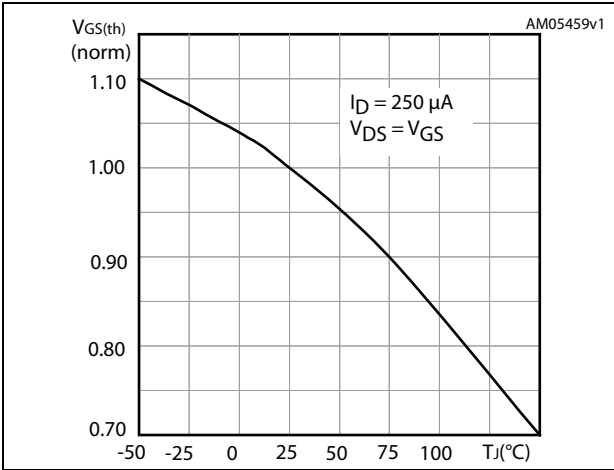


Figure 11. Normalized on-resistance vs temperature

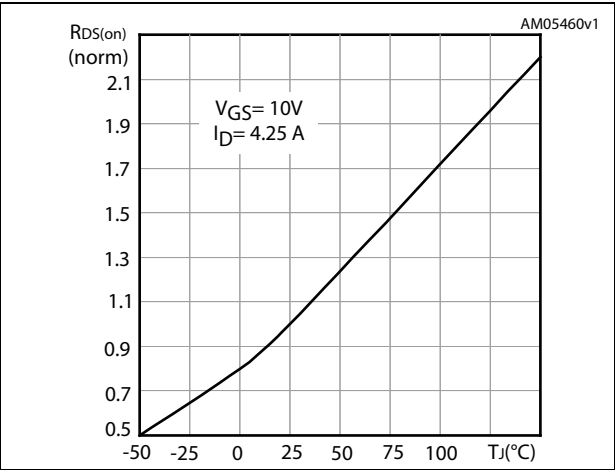


Figure 12. Source-drain diode forward characteristics

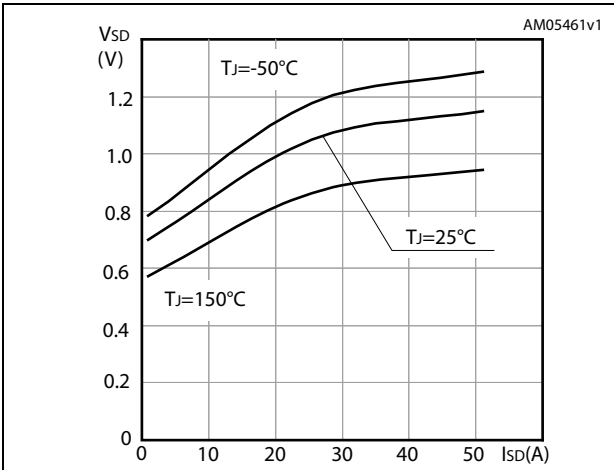


Figure 13. Normalized VDS vs temperature

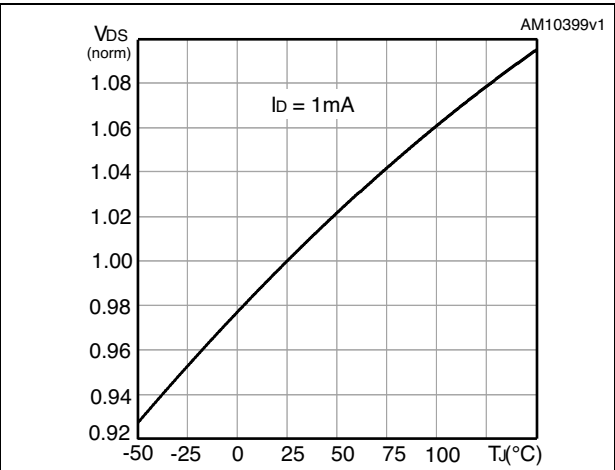
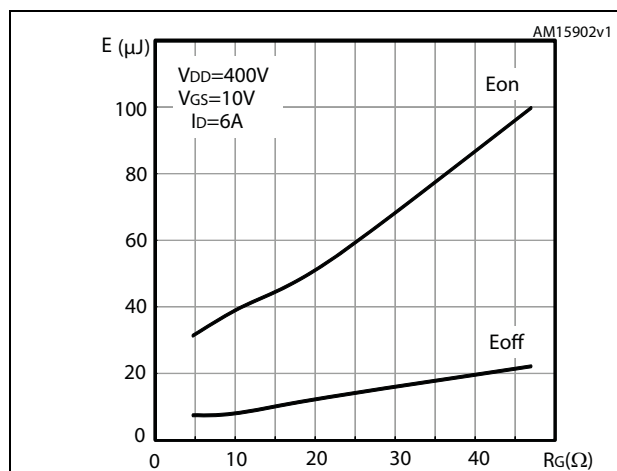
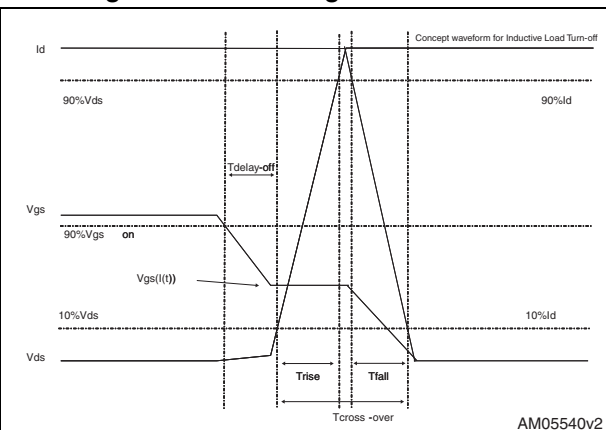
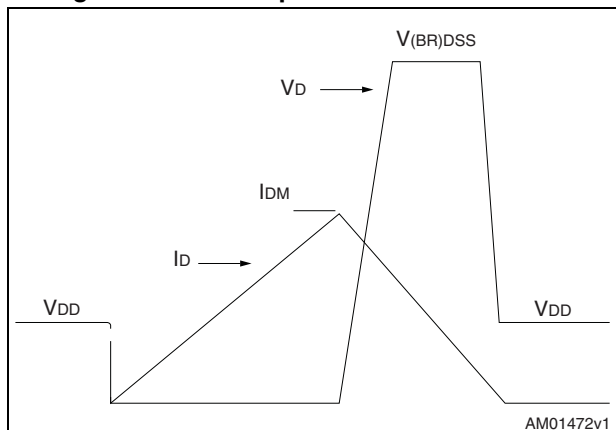
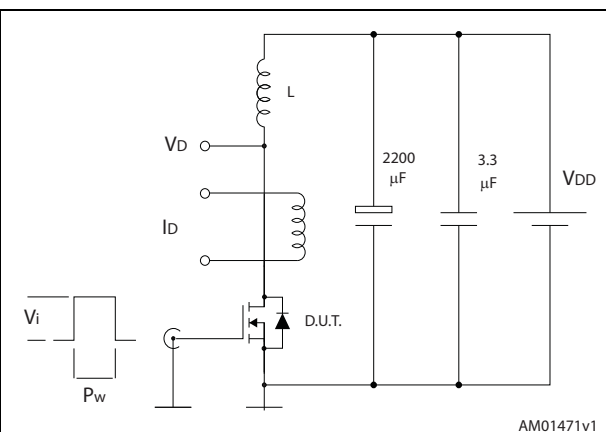
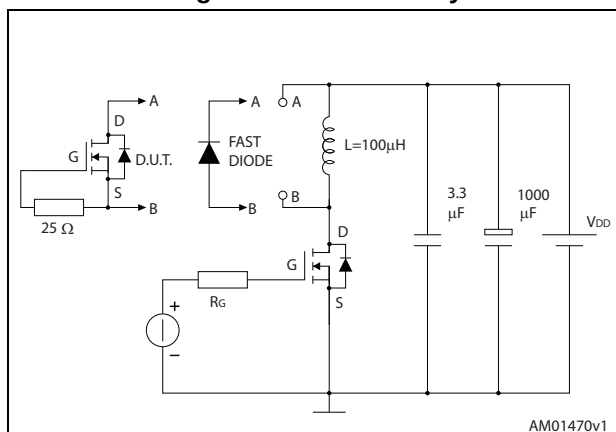
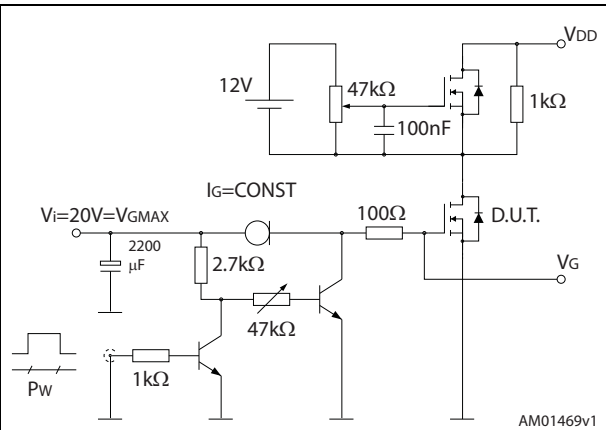
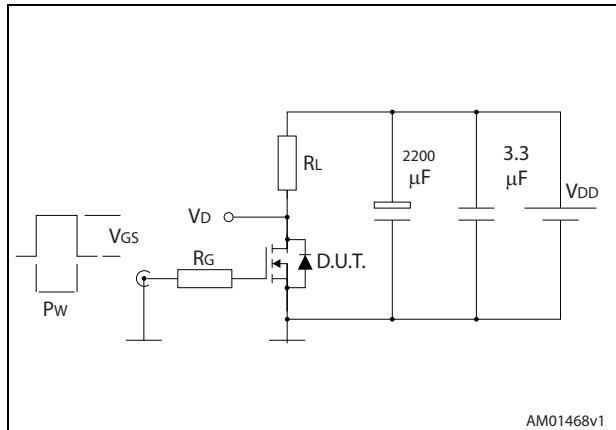


Figure 14. Switching losses vs gate resistance
(1)



1. E_{on} including reverse recovery of a SiC diode



4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

Table 8. PowerFLAT™ 5x6 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	5.95	6.15	6.35
D2	4.30	4.40	4.50
E2	3.10	3.20	3.30
e		1.27	
L	0.50	0.55	0.60
K	1.90	2.00	2.10

Figure 21. PowerFLAT™ 5x6 HV drawing

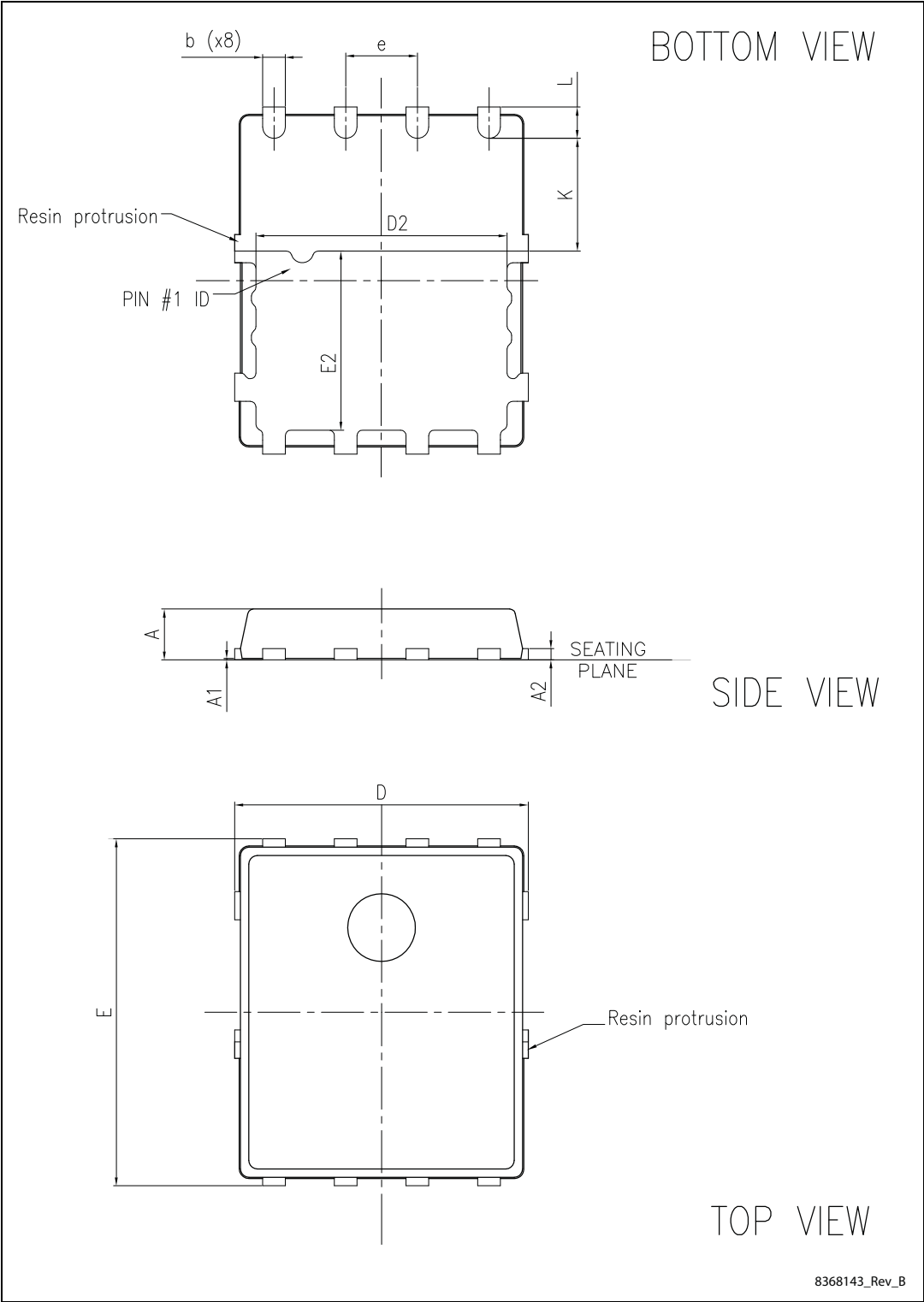
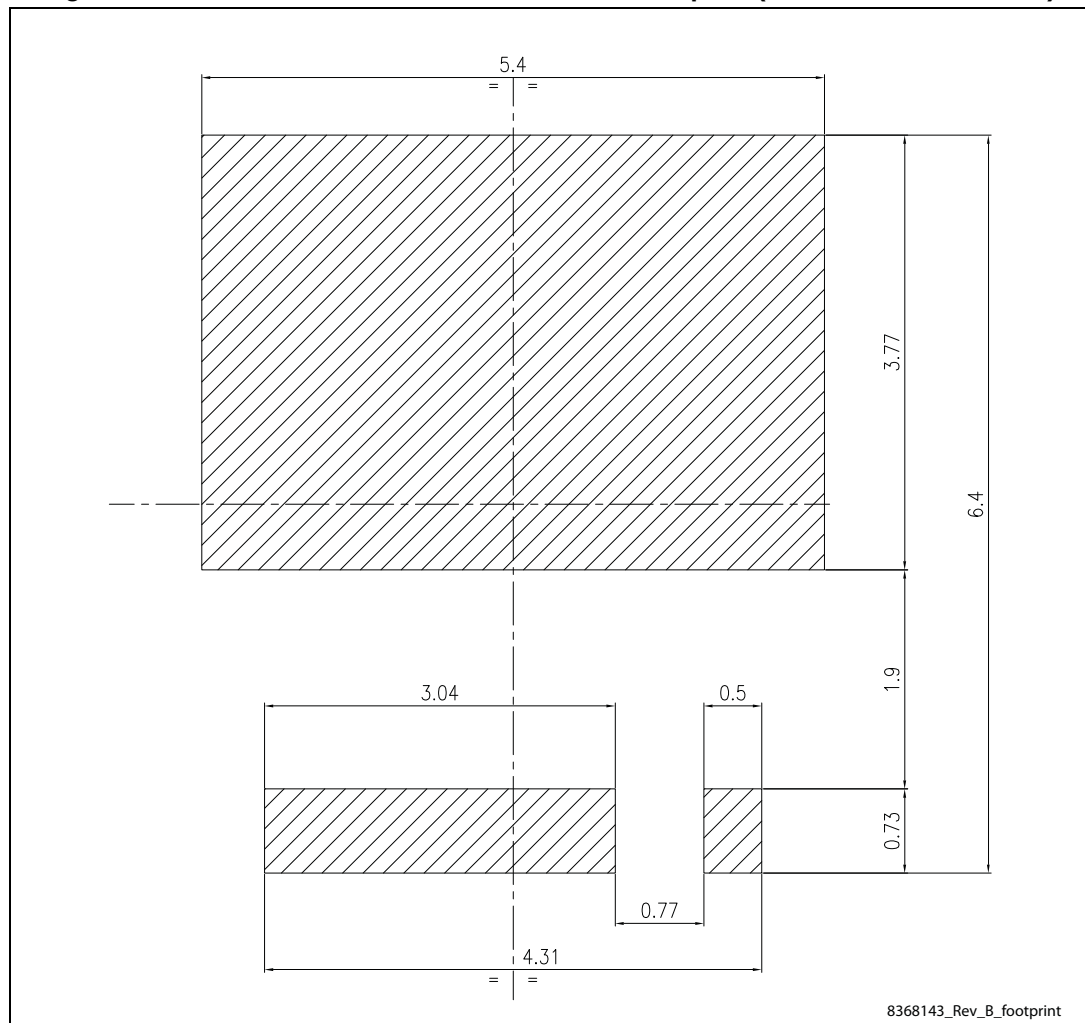


Figure 22. PowerFLAT™ 5x6 HV recommended footprint (dimensions are in mm)



5 Packaging mechanical data

Figure 23. PowerFLAT™ 5x6 tape^(a)

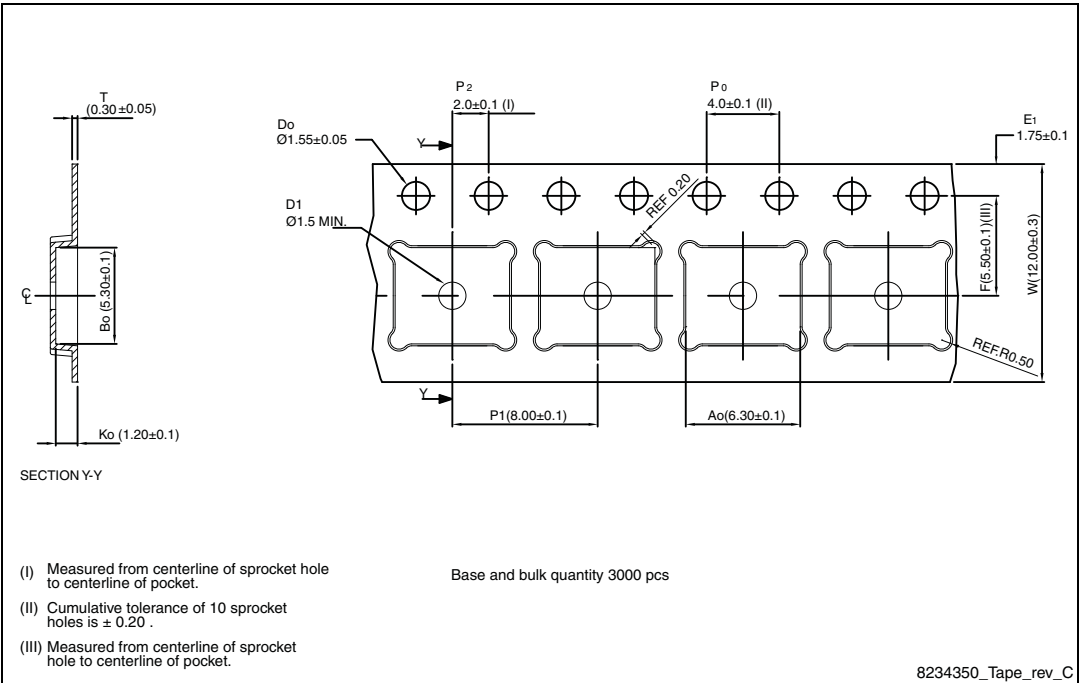
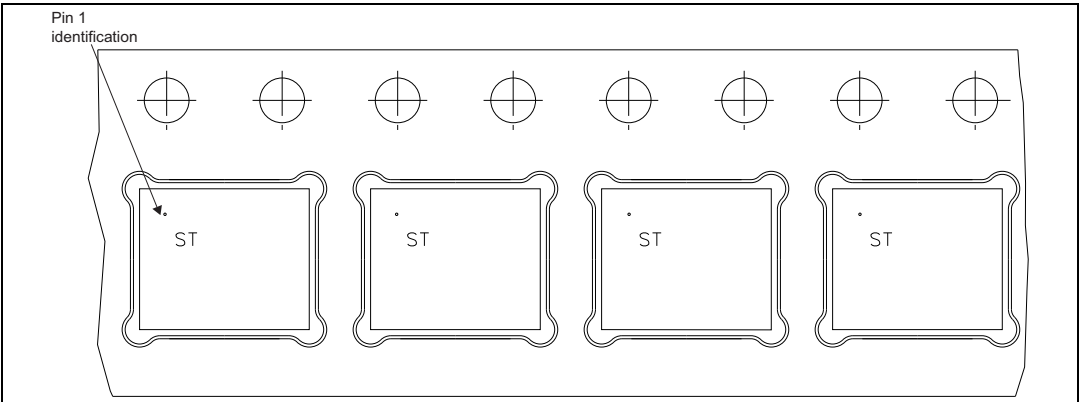
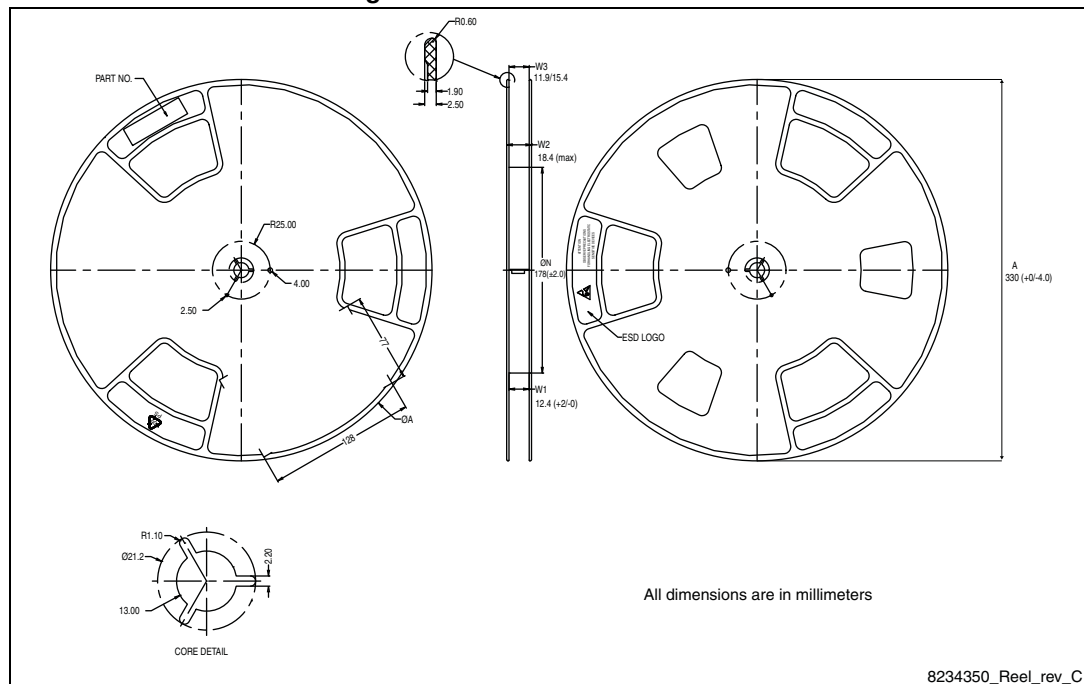


Figure 24. PowerFLAT™ 5x6 package orientation in carrier tape.



a. All dimensions are in millimeters.

Figure 25. PowerFLAT™ 5x6 reel



6 Revision history

Table 9. Document revision history

Date	Revision	Changes
30-Apr-2010	1	First release
22-Nov-2011	2	Document status promoted from preliminary data to datasheet: – Added Section 2.1: Electrical characteristics (curves) – Added Section 5: Packaging mechanical data Minor text changes
08-Jul-2013	3	– Changed: package – Modified: I_D (at $T_C=100\text{ °C}$), P_{TOT} value – Deleted: I_D at $T_{amb}=25\text{ °C}$ and 100 °C – Modified: note 1 and 3 in Table 2 , R_G in Table 5 , I_{SD} in Table 7 – Changed: figures in Section 2.1: Electrical characteristics (curves)
17-Jul-2013	4	– Minor text changes – Modified: Table 6: Switching times – Updated: Section 4: Package mechanical data

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